

S/N 09/551,027

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Wendell P. Noble et al.

Examiner: Michael Trinh

Serial No.: 09/551,027

Group Art Unit: 2822

Filed: April 17, 2000

Docket: 303.379US2

Title: **CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL
WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR**

TERMINAL DISCLAIMER

Commissioner for Patents
Washington, D.C. 20231

#15

I, Edward J. Brooks, III, am the attorney of record for the above identified patent application as evidenced by the Power of Attorney filed in the present application on April 17, 2000. I am making this petition on behalf of Micron Technology, Inc., the assignee of the present invention. As the attorney of record, I am empowered to act on behalf of the assignee and, in accordance with 37 C.F.R. § 1.321(b)(iv), to sign this terminal disclaimer.

Certificate Under 37 C.F.R. §3.73(b)

Your petitioner, Micron Technology, Inc., certifies that they are the owner of the entire right, title and interest in and to the above-identified patent application (Serial No. 09/551,027) and to U.S. Patent No. 6,156,604 and U.S. Patent No. 6,156,607. Your petitioner owns the entire right, title, and interest of these applications by nature of the assignments executed and filed for both of these applications. The assignment for U.S. Patent No. 6,156,604 was recorded on October 6, 1997 on Reel 8768, Frames 0729 - 0735, with the United States Patent and Trademark Office. The assignment for U.S. Patent No. 6,156,607 was recorded on October 6, 1997 on Reel 8765, Frames 0776-0782, with the United States Patent and Trademark Office. The above-identified patent application (Serial No. 09/551,027) is related to both U.S. Patent No. 6,156,604 and U.S. Patent No. 6,156,607.

The undersigned representative of the assignee has reviewed the evidentiary documents of title and certifies that to the best of assignee's knowledge and belief, title is in the assignee, Micron Technology, Inc., seeking to take the action set forth in this disclaimer.

09/551,027 ENTERED 09/25/01 09/25/01

10/16/01

213.01 01

RECEIVED

OCT 16 2001

TECHNOLOGY CENTER 2800
SPECIAL PROGRAM CENTER

RECEIVED
SEP 24 2001
TECHNOLOGY CENTER 2800

TERMINAL DISCLAIMER

Serial Number: 09/551,027

Filing Date: April 17, 2000

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Page 2

Dkt: 303.379US2

Terminal Disclaimer

✓ Your petitioner hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the above-identified patent application, which would extend beyond the expiration date of the full statutory term, as presently shortened by any terminal disclaimers, of U.S. Patent No. 6,156,604 and U.S. Patent No. 6,156,607. ✓ Petitioner hereby agrees that any patent so granted on the above-identified application shall be enforceable only for and during such period that the legal title to U.S. Patent No. 6,156,604 and U.S. Patent No. 6,156,607 and the legal title of the above-identified application and any patent granted thereon remain common, ✓ this agreement to run with any patent granted on the above-identified application and to be binding upon the grantee, its successors and assigns.

Limitations on the Disclaimer

Your petitioner does not disclaim any terminal part of any patent granted on the above-identified application prior to the expiration date of the full statutory term as presently shortened by any terminal disclaimer of U.S. Patent No. 6,156,604 and U.S. Patent No. 6,156,607 in the event that it later expires for failure to pay a maintenance fee, is held unenforceable, is found invalid, is statutorily disclaimed in whole or terminally disclaimed under 37 C.F.R. § 1.321(a), has all claims canceled by a reexamination certificate, or is otherwise terminated prior to the expiration date of its statutory term as presently shortened by any terminal disclaimer, except for the separation of legal title as stated hereinabove.

TERMINAL DISCLAIMER

Serial Number: 09/551,027

Filing Date: April 17, 2000

Title: CIRCUIT AND METHOD FOR A FOLDED BIT LINE MEMORY CELL WITH VERTICAL TRANSISTOR AND TRENCH CAPACITOR

Page 3

Dkt: 303.379US2

Fee Status

A check in the amount of \$110.00, which is required under 37 C.F.R. §1.20(d) to file a statutory disclaimer, is enclosed herewith. The Commissioner of Patents and Trademarks is hereby authorized to charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

WENDELL P. NOBLE ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

P.O. Box 2938

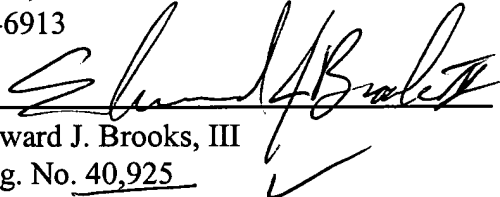
Minneapolis, MN 55402

(612) 373-6913

Date

9/19/2001

By



Edward J. Brooks, III

Reg. No. 40,925

"Express Mail" mailing label number: EL721276345US

Date of Deposit: September 19, 2001

This paper or fee is being deposited on the date indicated above with the United States Postal Service pursuant to 37 CFR 1.10, and is addressed to the Commissioner for Patents, Box CPA, Washington, D.C. 20231.